

Roadmap Details Latest Gas Purity Targets in Semiconductor Manufacturing

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Yield loss in the manufacturing of integrated circuits is caused by defects, faults, design, and variations in manufacturing conditions during processes such as implantation, etching, deposition, planarization, cleaning, and lithography. Contaminants in the materials used and the wafer environment are primary causes of defects and process variations that compromise yield.

After much delay in the internal review process, the approved chapter on “Yield Enhancement” (YE) in the 2009 Edition of the International Technology Roadmap for Semiconductors (ITRS) finally became available on the ITRS web site in May. Most chapters have been online by January and February of this year, following the official release of the Roadmap in December 2009. The remaining chapters on “Interconnect” and “Assembly and Packaging” came online in June 2010.

Current and earlier editions of the ITRS, figures, tables, and corresponding supplemental materials can be viewed or downloaded at www.itrs.net. Please refer to the chapter on Yield Enhancement for in-depth information on the topics discussed here.

The YE chapter focuses on three concerns in front end processes: yield model and defect budget; defect detection and characterization; and wafer environment contamination control. The last issue relates to the latest limits for critical fluid and gas impurity levels in the fabrication of electronic devices with exponentially decreasing minimum feature sizes.

On the subject of technology metrics, the 2009 ITRS re-emphasizes the need to track technology trend targets as annualized targets for each specific product (DRAM, MPU/ASIC, and Flash) separately through the 15-year Roadmap projection (“Near-term years” 2009–2016; “Long-term years” 2017–2024). There has been much confusion as semiconductor companies refer to “technology nodes” and timing, which do not necessarily align with the ITRS definitions and specific targets. The term was originally used in previous editions of the ITRS in an attempt to provide a single, simple indicator of overall industry progress in IC feature scaling, specifically defined as the smallest half-pitch of contacted metal lines on any product. Historically, DRAM has been the product, where one half the average of the width and the space in between metal lines connecting bit cells in a DRAM used to exhibit the tightest contacted metal pitch, and “set the pace” for the ITRS technology nodes. Since different IC parameters are now believed to scale at different rates and the timing of a technology cycle is unique to a particular product, it is misleading to continue with the DRAM interconnect M1 half-pitch as a single highlighted driver of scaling and definition of a technology cycle.

Beginning with the 2007 ITRS, the International Roadmap Committee has eliminated references to the term and has adopted the year of first production as the only standard header, with multiple product feature sizes as historical indicators of IC scaling. As such, the term “product generation” is no longer used interchangeably with “technology cycle.” Another source of confusion for gas users, that led to ambiguous discussions of gas quality in a process stream, is the different locations where gas impurity can be measured. The three primary sources of process environment contamination are: impurities in the process materials as

supplied; the delivery system or the process itself; and decomposition. These sources can be found throughout the process stream, from the delivered gas to the wafer surface. In order to clarify the location of major gas handling nodes, the ITRS defines the critical locations in the pathway as the point of supply (POS), point of delivery (POD), point of connection (POC), point of entry (POE), point of use (POU), and point of process (POP) (see table). The ITRS targets for wafer environmental contamination control refer to gas attributes at these different nodes, namely interfacial points of process materials with equipment along the manufacturing pathway.

Definition for the Different Interface Points for Gases

	POS Point of Supply	POD Point of Delivery	POC Point of Connection	POE Point of Entry	POU Point of Use	POP Point of Process
	<i>Delivery point of gas supplier</i>	<i>Outlet of central facility system</i>	<i>Sub-main or valve manifold box or post(VMB/VMP) take off valve</i>	<i>Entry to equipment or sub-equipment</i>	<i>Entry to the process chamber</i>	<i>Contact with wafer</i>
Cleanroom and airborne molecular contamination (AMC)	Outside air	Outlet of make-up air handling unit	Outlet of filters in cleanroom ceiling	Inlet to mini-environment or sub-equipment for AMC, outlet of the tool filter for particles	Gas/air in vicinity to wafer/substrate	Wafer in production
Bulk gases	Bulk gas delivered on site or gas generator	Outlet of final filtration/purification	Outlet of sub-main take off valve or VMB valve	Inlet of equipment/sub-equipment	Inlet of chamber (outlet of mass flow controller)	Wafer in production
Specialty gases	Gas cylinder or bulk specialty gas systems	Outlet of final filtration of gas cabinet	Outlet of VMB valve	Inlet of equipment	Inlet of chamber (outlet of mass flow controller)	Wafer/substrate in production (airborne molecular contamination/surface molecular contamination)

Source: Table YE1, "Yield Enhancement," International Technology Roadmap for Semiconductor, 2009 Edition

Since it is difficult to measure gas impurities at the POP, where process performance can be correlated directly with the quality of the gas, measurements at the POU provide the most direct information on the gas entering the process chamber. In reality, even measurements at the POU are not available for many of the common processes. The values stated in the ITRS are meant to represent those at the POE, defined as the inlet to the process tool. The targeted levels can be reached either by bulk delivery of a gas with the requisite purity or through the use of local filtration and purification. The ITRS states that the prevailing approach is to seek POC

levels that are adequate for the process and employ purifiers to obtain targeted gas purity at the POE/POU.

Historically, as IC design features decreased in size, lower and lower levels of contaminants in process gases could lead to failure-causing defects in the device. Acceptable levels of contamination decreased with device geometry as processes for each generation of technology became more and more sensitive to the presence of moisture, oxygen, hydrocarbons, metallic impurities, etc. As a result, earlier editions of the Roadmap deemed it necessary to stringently increase gas purity as DRAM ½ pitch progressed toward 90 nm and below. This required improving control limits for contamination in gases, chemicals, air, precursors, ultrapure water, and substrate surface cleanliness. Ensuring high gas purity from the supplier, during transit and storage, as delivered, and minimizing variations in purity during manufacturing were key to yield management.

Critical processes such as lithography demand ultra-high purity gases that used to present a cleanliness challenge to suppliers and users. As electronic gas suppliers rose to the challenge and delivered gases with impurities in the ppm and ppb levels, it became evident that currently-achievable purity levels for gases and chemicals used in semiconductor manufacturing could be sufficient for multiple generations. Maintaining that level of purity rather than reducing gas specifications is now the main focus of newer contamination control programs. In addition to the use of gas filters as close as possible to the POU, gas purifiers has become essential to remove contaminants downstream of the POS that either enter the gas distribution system during maintenance or cylinder changes, through leaks, or are created during manufacturing. Particulates from plasma processing, cleaning, and the gas delivery system, as well as impurities released by reactions of wet chemicals can be generated in situ and gas purity can vary in the process stream. Local purifiers are recommended to ensure ultimate purity (impurities in the ppb to ppt range) at the POU.

By the year 2007, there was little objective evidence to support the need for order-of-magnitude improvements in impurity levels of bulk gases to meet post-45nm design rules. As a result, the 2007 Edition of the ITRS was modified from the 2005 Edition to remove many of the step improvements previously scheduled for future manufacturing nodes, except for very special applications where extraordinarily higher purities are critical and special purity grades or additional purification are identified. Some bulk gas requirements, such as the criteria to control Ar as an impurity, were also relaxed. In addition, detecting organic refractor components at the 0.1 ppbv level in nitrogen and helium has become a challenge using existing analytical methods. Similar relaxation of purity requirements for specialty gases appeared in the 2007 Edition and has remained unchanged in the 2009 Edition. Both editions show more tolerance for impurities in corrosive etchants and deposition gases for sub-45nm design rule manufacturing. In addition to more comprehensive classification of bulk and specialty gases, the contaminant values in etchants, dopants, deposition gases, and gases used in laser applications are provided in a detailed supplemental spreadsheet to reflect the increasing number of materials used and to better delineate the processes for which they are used. The supplement also includes requisite purity

levels for novel materials used for metal oxides, CMP slurries, low/high k dielectric materials, precursors, and barrier/conductor metals.

The 2009 Edition of the Roadmap continues to show an essentially flat gas and liquid chemical purity trend, although it is likely that specific process steps (such as low temperature epitaxy and its cleaning gases) may require higher purity. The ITRS expects this to be reflected in wider use of the best-available purity rather than substantial improvements. Yield improvements may be achieved more by reducing fluctuations in purity than by reduction of average contamination levels. There is, therefore, a need for improved statistical process control (SPC) of incoming materials to reduce variation at the POS, as first identified in the 2005 Edition. It is more challenging to maintain POS purity levels for chemically-reactive specialty gases throughout delivery to the POP. Therefore, gases such as anhydrous hydrogen chloride (AHCl) are expected to be among the first targeted for SPC at the POS. Inconsistencies in purity levels at the POU may remain due to variations in downstream contributions and POU purification would be necessary to minimize these variations.

G&I has covered the topic of gas purifiers and AHCl in recent months (to view previous Newsletter features see “Newsletter Features Archive” and <http://www.gasesmag-digital.com/gasesmag/20100506#pg4>) Watch out for new articles on how POU purifiers can be used to meet IC contamination control requirements in upcoming issues of the Magazine and Newsletter.